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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/598,903	09/14/2006	Hiroyuki Fukusako	10873.1953USWO	1844

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/598,903	FUKUSAKO ET AL.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8* is/are pending in the application.

4a) Of the above claim(s) *2-6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Serial Number: 10/598903 Attorney's Docket #: 10873.1953USWO
Filing Date: 9/14/2006; claimed foreign priority to 3/16/2004

Applicant: Fukusako et al.

Examiner: Alexander Williams

This application is a 371 of PCT/JP05/04349, filed 3/11/2005.

Applicant's Amendment filed 7/7/08 to election of Species IV, figure 7 (claims 1, 7 and 8), filed 2/21/2008, has been acknowledged.

This application contains claims 2 to 6 drawn to an invention non-elected without traverse.

Claims 7 has been cancelled.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 and 8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirohashi Osamu (Japan Publication # 2001-326879) in view of Maki Toshimitsu (Japan Application # 11-284113) and further in view of Narayan et al. (U.S. Patent # 5,721,602).

Hirohashi Osamu (figures 1 and 2) show a driver module structure comprising: a flexible circuit board **11** provided with a wiring pattern **17**; a semiconductor device **12** mounted on the flexible circuit board; and an electrically conductive heat-radiating member **13** joined to the semiconductor device, wherein the wiring pattern comprises a ground wiring pattern **16**, the flexible circuit board has a cavity that exposes a portion of the ground wiring pattern, and the exposed portion of the ground wiring pattern and the heat-radiating member are connected to establish electrical continuity via a member that is fitted into the cavity. Osamu show the features of the claimed invention as detailed above, but fail to explicitly show the cavity is a through hole penetrating the ground wiring pattern, a portion of the ground wiring pattern on an opposite side from the heat-radiating member is exposed, and the member fitted into the cavity is a fastener for fastening the flexible circuit board and the heat-radiating member.

Toshimitsu is cited for showing a heat radiation mechanism for a semiconductor integrated device. Specifically, Toshimitsu (figures 1 and 2) discloses the cavity is a through hole **34** penetrating the ground wiring pattern, a portion of the ground wiring pattern **32** on an opposite side from the heat-radiating member **20,21** is exposed, and the member fitted into the cavity is a fastener for fastening the flexible circuit board **30** and the heat-radiating member for the purpose of providing a heat dissipation mechanism capable of efficiently the heat generated in a semiconductor integrated device even if

a space can be ensured for mounting a heat sink directly on the semiconductor integrated circuit device.

The combination of Osamu and Toshimitsu fail to explicitly show the member fitted into the cavity is a screw for fastening the flexible circuit board and the heat-radiating member. It would have been an obvious matter of design choice to use various forms of a fastener including a screw, since Applicants has not disclosed that since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

Narayan et al. s cited for showing a mechanical packaging and thermal management of flat mirror arrays. Narayan et al. (figures 1 to 6) specifically figure 4 discloses a screw **34** for fastening the flexible circuit board **20** and the heat-radiating member **30** for the purpose of providing a heat dissipation mechanism capable of efficiently the heat generated in a semiconductor integrated device even if a space can be ensured for mounting a heat sink directly on the semiconductor integrated circuit device.

Detailed Description Text - DETX (14):
Referring now to FIG. 4, a cross-sectional view of the liquid crystal display element 12 and the substrate holder 20 having a heat sink device 30 coupled to the rear side of the holder 20, and being mounted to a wiring board 40 is provided. As described above, the element 12 is disposed on the optically flat substrate 14, which is in turn coupled to the substrate holder 20 via an adhesive thermal paste 32. The substrate holder 20 is coupled to a wiring board 40 by a set of coupling screws 34 which are disposed through the wiring board into the screw holes 26 of the holder 20. The wiring board includes cut-out sections formed therein (see FIG. 5), about which the substrate holders 20 are coupled, and in which cut-out sections the display elements 12 are positioned so that they are in light

receiving position with the remainder of the optical elements in the display device.

Detailed Description Text - DETX (15):

Referring now to FIG. 5, the wiring board 40 is shown, having a liquid crystal element 12 mounted in a cut-out section 42 thereof, is shown in a perspective view. The region of the wiring board 40 which is adjacent to the cut-out section 42 includes a plurality of electrical connection pads to which the proper electrical connections (not shown) may be made to provide coupling to the driver chips 44 to drive the element 12. In the area surrounding the cut-out section 42, screw holes 46 are further provided which are mateable to the substrate holder 20 by screws 34, as described above.

Detailed Description Text - DETX (16):

In order to make the electrical connection of the driver chips 44 to the wiring board 40, the driver chips 44 are first attached to the semiconductor wafer 4 which is known in the art. Then, the element 12, with driver chips 44 attached, must be precisely oriented on the wiring board 40. In this aligned position the electrical connection of the driver chips 44 to the wiring board 40 is made. Referring now to FIG. 6, an alignment fixture 50, which is mountable to the rear of the substrate holder 20, as described above, is shown in a perspective view using the alignment fixture 50 while holding the wiring board 40 stationary. Once the substrate holder 20 and the element 12 mounted therein with driver chips 44 attached have been placed against the wiring board 40, with the driver chips 44 aligned to the electrical connection pads on wiring board 40. It is understood that the alignment fixture 50 may be of a slightly different configuration depending on the configuration of the device forming the electrical connections. For example, the wiring board and element assembly may be held horizontally instead of vertically, as shown, or the assembly fixture may contain rotary capability.

Detailed Description Text - DETX (18):

In order to mount a plurality of liquid crystal elements 12 in proper alignment with remote optical elements, for example three elements each dedicated to a specific color and are aligned to projection optics to form a single color image, each assembly of liquid crystal elements 12 with driver chips 44 and wiring board 40 attached (shown as element 54 in FIG. 5) must be

precisely oriented to the projection optics. With an alignment fixture 50 attached to each of the several assemblies 54, such alignment can be achieved.

Detailed Description Text - DETX (26):
Referring now to FIG. 8, the rear surface of the wiring board 40 is shown, with the heat sink 30 coupled to the back of the substrate holder 20, as was illustrated in a side view in FIG. 4. The heat sink 30 is coupled to the rear of the wiring board 40, after the proper positioning of the assembly 54, via screws 52. The holes in the wiring board 40, through which the screws 38 are placed, may be the same as the holes as were utilized to couple the alignment fixture 50 thereto, otherwise a separate set of holes may be provided.

Detailed Description Text - DETX (28):
The process of assembling and aligning the structure 7, once fabricated, with the remaining optical and electrical elements of the display device comprises: (1) attaching driver chips and/or flexible circuitry to the semiconductor wafer; (2) attaching the element to a substrate holder; (3) loosely mounting the substrate holder to a wiring board, such that the structure is positioned in a cutout section of the board; (4) utilizing an adjustment fixture, aligning the driver chips and/or flexible circuitry to the bonding pads on the wiring board; (5) connecting the driver chips and/or flexible circuitry to the wiring board; (6) tightening the mounts of the substrate holder to the wiring board; (7) utilizing another adjustment fixture, temporarily mounted in contact with the element, the substrate holder, and the wiring board, for the purpose of adjusting the relative orientation of the liquid crystal element with respect to the other optical elements of the device; (8) attaching the assembly to a mounting device; and (9) coupling a heat sink to the rear of the substrate holder for the purposes of dissipating as much of the thermal build-up in the element as possible.

8. The driver module structure according to claim 7, the combination with Toshimitsu show wherein the exposed portion of the ground wiring pattern and the fastener are connected via an electrically conductive bonding material.

Therefore, it would have been obvious to one of ordinary skill in the art to use Narayan et al.'s screw and Toshimitsu's heat radiating member in the through hole to modify Osamu's heat radiating member for the purpose of providing a heat dissipation mechanism capable of efficiently the heat generated in a semiconductor integrated device even if a space can be ensured for mounting a heat sink directly on the semiconductor integrated circuit device.

Response

Applicant's arguments filed 7/7/2008 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The insertion of Applicant's additional claimed language, for example, "in claim 1" cause for further search and consideration to make this action final.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. э 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. э 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. э 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

The listed references are cited as of interest to this application, but not applied at this time.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272 1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Alexander O Williams/
Primary Examiner, Art Unit 2826

AOW
8/15/2008